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•	INFORMATIO			Application Number	09/963,735	1		
	" STATEMENT!	BY APPLI	CANT	Filing Date	09-27-2001	Nov	一	
Date Submitted: November 13, 2002 (use as many sheets as necessary)				First Named Inventor	Nobuo FUDANUKI	13 2002	+	
				Group Art Unit	2819	2	#	
				Examiner Name	Unassigned	(F)	_	
Sheet	1	of	1	Attorney Docket Number	016910-0476	RADEMIN		

U.S. PATENT DOCUMENTS						
Examiner Initials*		U.S. Patent Document			Date of Publication of	Pages, Columns, Lines,
	Cite No. <sup>1</sup>	Number	Kind Code <sup>2</sup> (if known)	Name of Patentee or Applicant of Cited Document	Cited Document MM-DD-YYYY	Where Relevant Passages or Relevant Figures Appear

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Examiner Initials*	Cite No.1	Offic	Foreign Patent [ e <sup>3</sup> Number <sup>4</sup>	Occument Kind Code <sup>b</sup> (if known)	Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T⁰
W	A1	JP	1-100942		Semiconductor Integrated Circuit	04-19-1989		Х
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		OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>6</sup>		
ar A3	А3	"A Versatile VLSI Design System for Combining Gate Array and Standard Cell Circuits on the Same C Robert Homung, Martine Bonneau and Bernard Waymel, IEEE 1987 Custom Integrated Circuits Conference.			

Examiner Signature	00 N	W.	Date Considered	7/1/02	

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